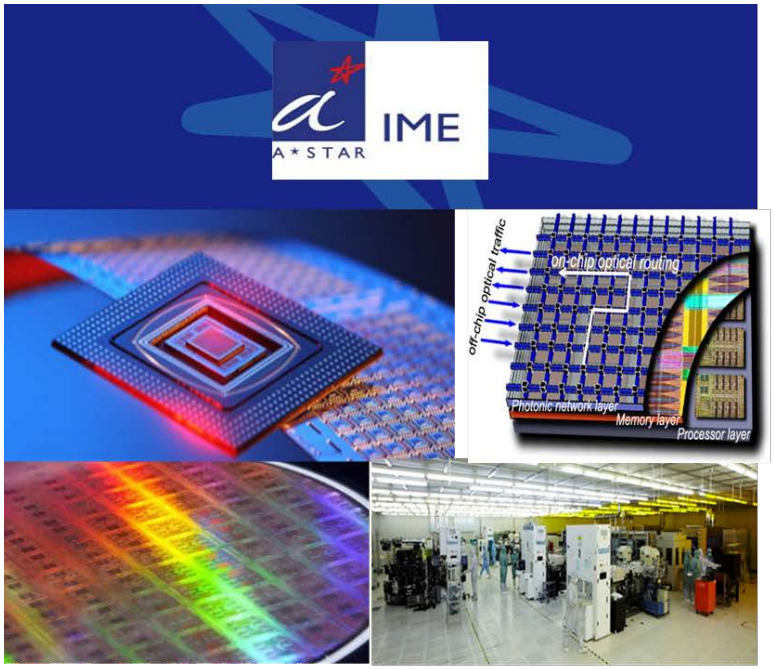




# Life After Moore's Law @ A*STAR

**Prof. Dim-Lee Kwong**

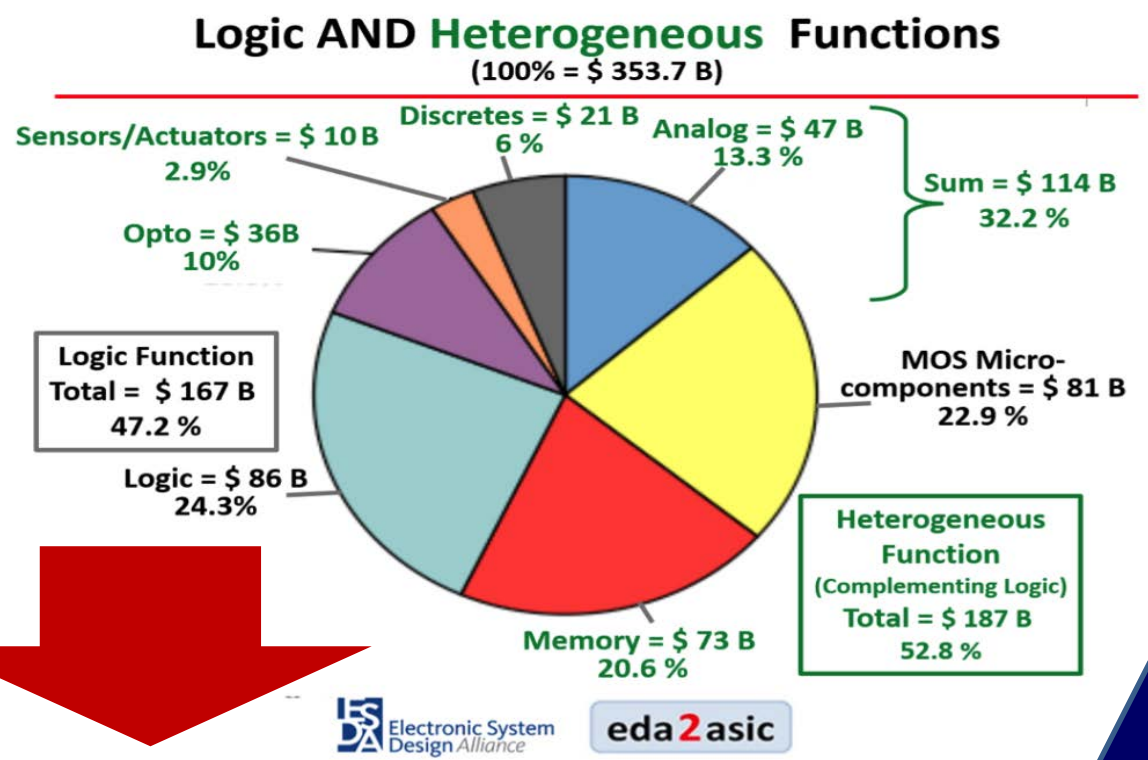
**Executive Director, Institute of Microelectronics (IME)**

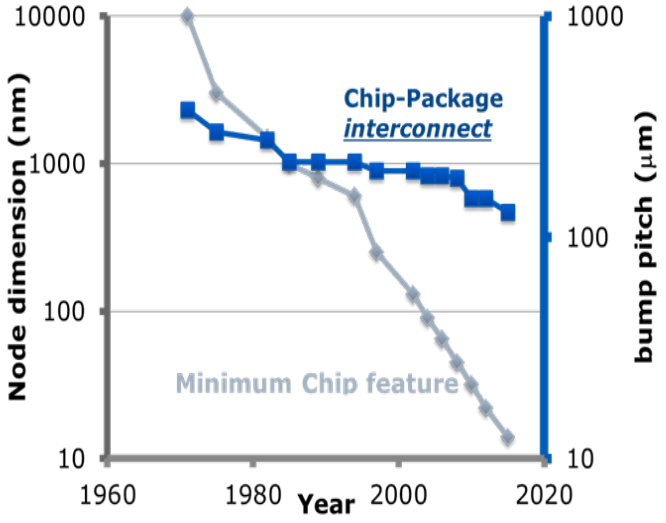
**Executive Director, Institute for Infocomm Research ($I^2R$)**

CREATING AN INNOVATION ECONOMY

Agency for Science, Technology and Research
SINGAPORE

# Paradigm Shift in Semiconductor Industry
## *Heterogeneous Integration for System Scaling*

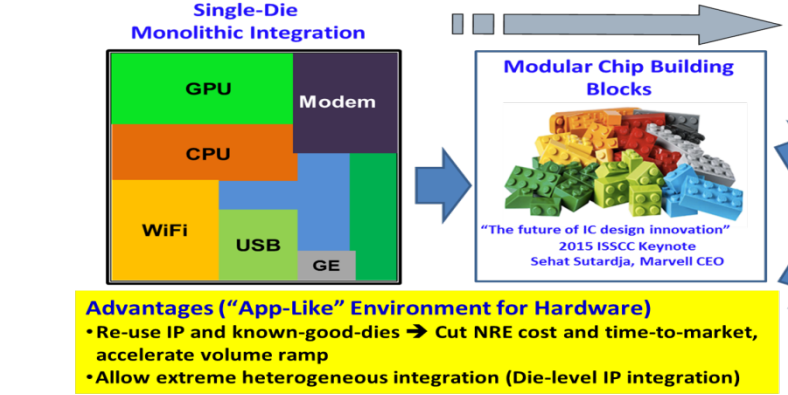


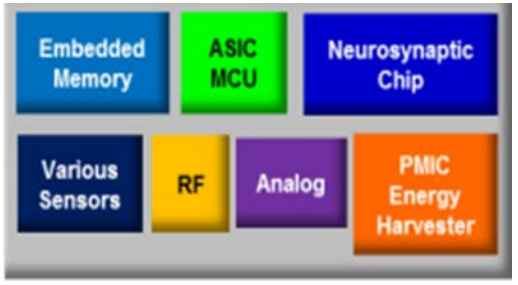

- Packaging has not scaled much in the last 40 years compared to transistors
  - Scaling the package will be central for the next decade

Electronic System Design Alliance

eda2asic




**Advantages ("App-Like" Environment for Hardware)**
- Re-use IP and known-good-dies ➔ Cut NRE cost and time-to-market, accelerate volume ramp
- Allow extreme heterogeneous integration (Die-level IP integration)


**Multi-Die Packaging**

ONOMY

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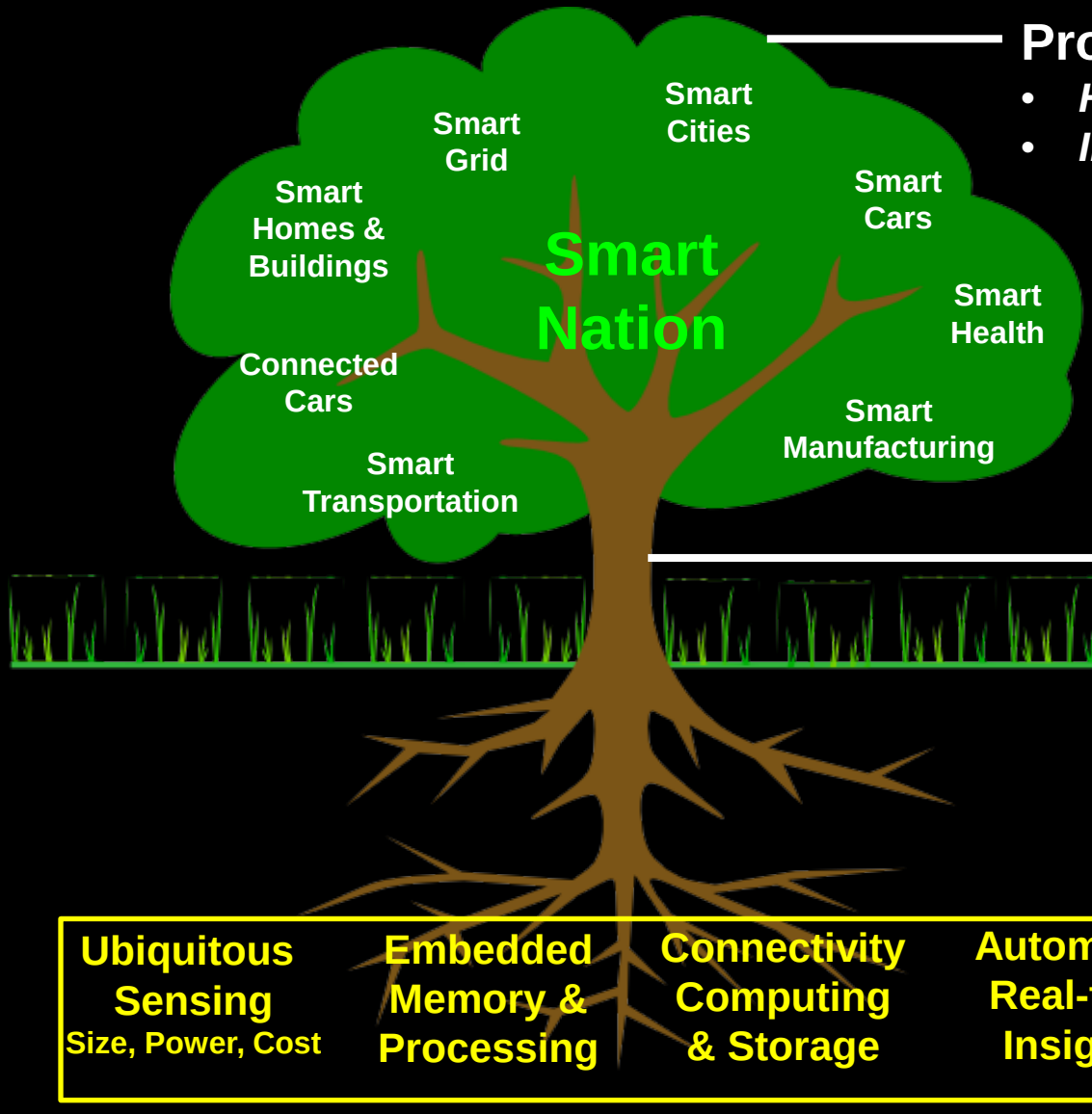
# A*STAR's Strategy for *Solution-Based* IoT

## Hardware & Software Integration for System Design Enablement

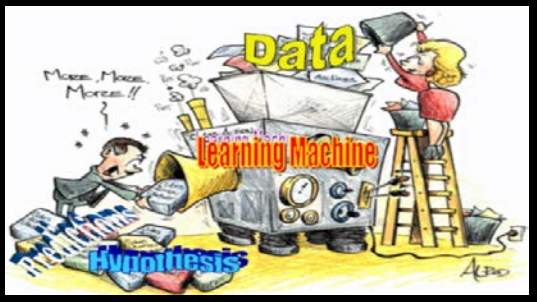



**Products & Services**

- *Huge opportunities for start-ups*
- *Integrated fabless manufacturing model*


**Multi-Dies FOWLP**

**Security (IME & I2R)**
(*Device, Networking, Software*)




| Ubiquitous Sensing | Embedded Memory & Processing | Connectivity Computing & Storage | Automated Real-time Insights |
|---|---|---|---|
| Size, Power, Cost | | | |

**Software (I2R)**

**Hardware (IME)**

# IME's Heterogeneous Integration R&D & Infrastructure

## Science Park II

200/300 mm "More than Moore"

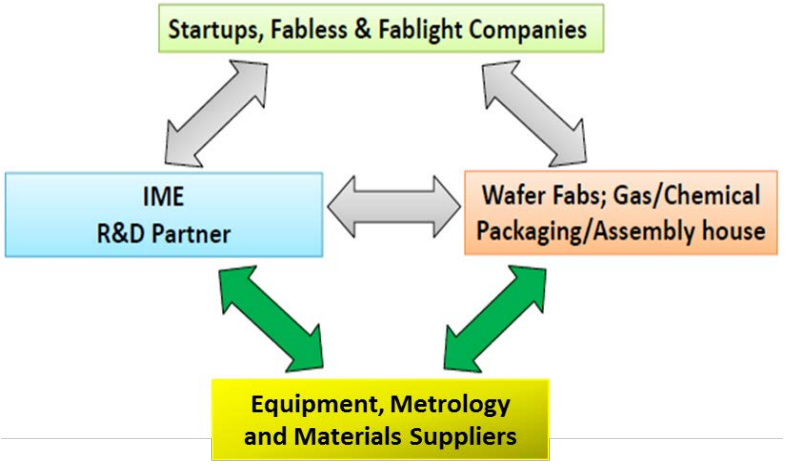
300 mm Multi-Dies Fan-Out WLP Development Line

300 mm 2.5D/3D Interposer

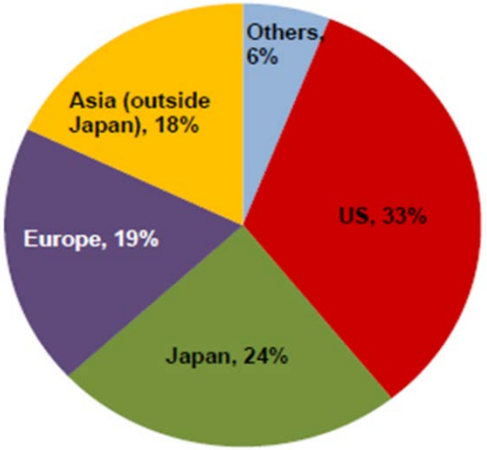

## Fusionopolis 2

300 mm Industry Joint Labs

- Advanced Lithography
- Wafer-Level Packaging
- Metrology
- Thin film magnetic and PZT




- Complementary IP, Capabilities, Talents
- Earlier, Faster, Cheaper




More Than Moore: *Heterogeneous* Components
*Functionality and Embedded Integration*

*Heterogeneous* System Integration & Miniaturization
*Performance (I/O Bandwidth), Power, Form Factor, Cost*

- Technology platform
- Industry pre-competitive consortia
- >100 global customers/partners

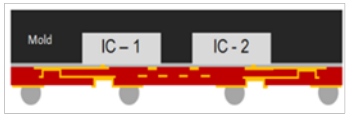
**World leading infrastructure bridging R&D and manufacturing**

# IME's Multi-Die FOWLP Development Line

**System design, integration flow, equipment, metrology, materials**

Carrier Wafer Preparation → Front Side RDL Formation → Cu Pillar Formation → Back Side RDL Formation → Wafer Level Molding → Chip-to-Wafer Bonding → Carrier Removal, Bumping, Dicing

**Integrating the entire supply chain partners & resources to drive solutions**





**Develop "must have" baseline platform**

- Pre-competitive consortium approach
- *Fabless, IDM, foundry, OSAT , EDA as Core members*
- Demonstrate solution candidates, ready supply chain and influence technology roadmap

**Develop *customized* integration flow with *selected* local manufacturing partner for *specific* product**

**Foundry OSAT**

**Deliverables**: Data required to

- make strategic decisions early on processes, tools, materials, architecture
- estimate the manufacturability, variability, reliability, cost and performance attributes of a target platform in order to reduce the risks of adoption

A*STAR IME


Thank You!